Overview of the ATLAS Pixel Electronics

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Goal: provide an overview of pixel electronics. This talk will be followed by two technical talks on the major pixel IC's: the FE chip and the MCC chip.

Module design concept

- Components of the module

Electronics required

- Front-end chips
- Module Controller chip
- Prototype Results

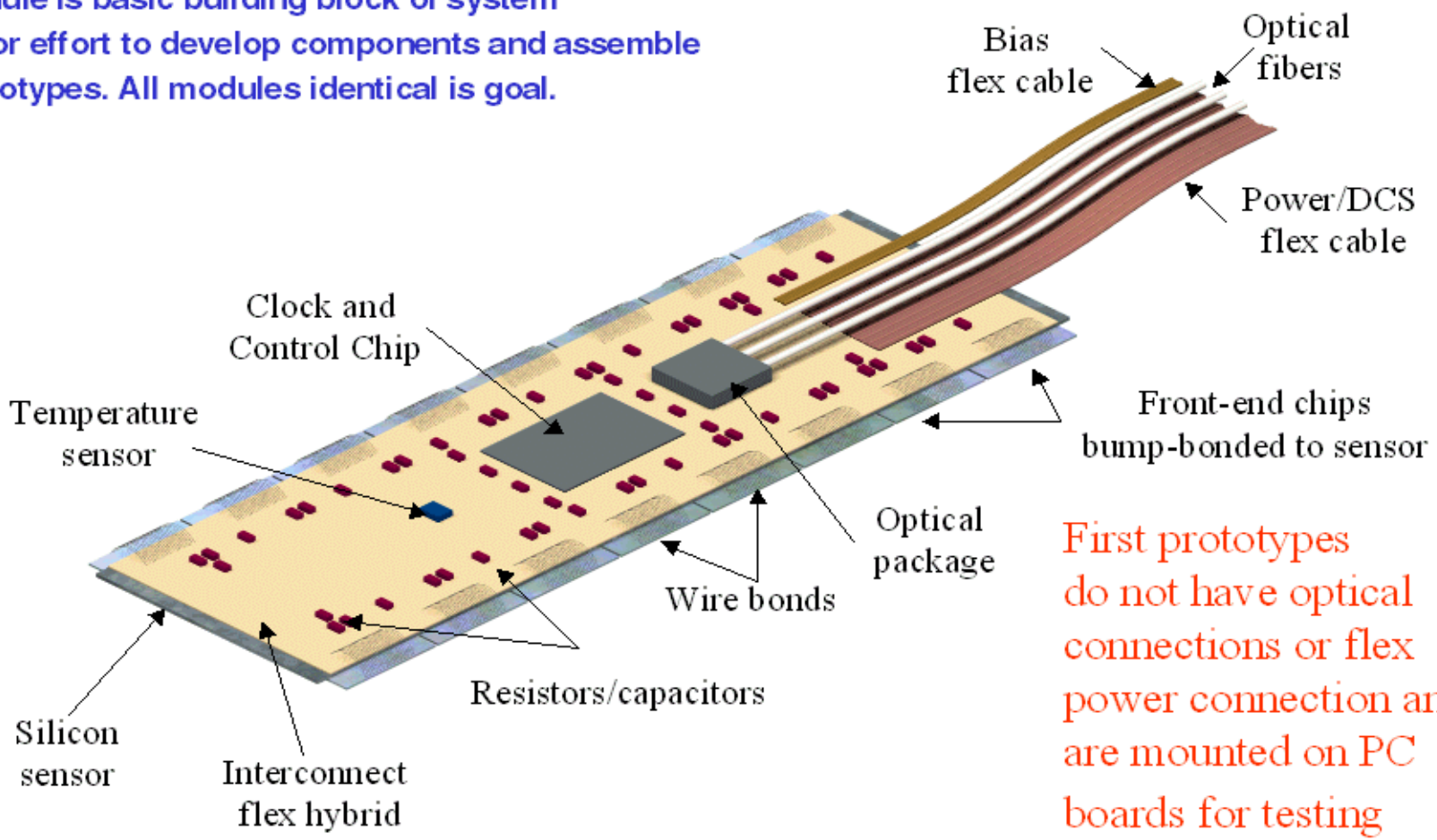
Scope and Schedule of Electronics Activities

Basic Components of Pixel Tracker

Modules placed on a mechanical support/cooling structure:

- Silicon sensor with 16 FE chips, controller chip, power cable and opto-link

Module is basic building block of system
Major effort to develop components and assemble prototypes. All modules identical is goal.



First prototypes do not have optical connections or flex power connection and are mounted on PC boards for testing

- Each module has active area of 16.4x60.8mm and includes 46K pixels of size 50μ x 400μ each.

FE Electronics Concepts

System Design:

- **Pixel Array:** FE chip of 7.4 x 11.0mm die size with 7.2 x 8.0mm active area. The chip includes 2880 pixel channels, internal analog bias control via serial commands, and complete zero-suppressed readout with serial 40 Mbit/s data output. The set of hits from a 25ns crossing is “requested” by sending a LVL1 signal with the correct latency, and the FE chip then transmits the corresponding digital hits autonomously. This is a full-custom chip with about 800K transistors.
- **Module Controller:** Collects data from 16 FE chips and implements a silicon event builder. Performs basic integrity checks and formats data, also implements module level command and control. This is a synthesized chip, with embedded custom blocks and about 400K transistors.
- **Opto-link:** Multiplexed clock/control sent over 40 Mbit/s link to module, data is returned on one or two 80 Mbit/s data links. Transmitters are VCSELs, receivers are epitaxial Si PIN diodes. There are two small optolink chips with LVDS interfaces to support these functions.
- **Power Distribution:** Significant ceramic decoupling used on module. Flex power tape used to reach services patch-panels on cryostat wall (1.5m) followed by round cable to later transition on back of calorimeter, then conventional cables to USA15 cavern (total distance as large as 140m).

Electronics Challenges and Requirements

Most difficult challenges are in FE chips:

- **Radiation Dose:** Operate properly after total dose of 50 MRad (nominal ATLAS 10 year dose). Also cope with expected leakage currents from sensors of up to 50nA per pixel. For the B-layer, this corresponds to a lifetime of about 2 years at design luminosity.
- **Low noise:** Operate with low noise occupancy (below 10^{-6} hits/pixel/crossing) at thresholds of about 3Ke with good enough timewalk to have an "in-time" threshold of about 4Ke (hit appears at output of discriminator within 20ns of expected time). This requires a small threshold dispersion (about 200e) and low noise (about 300e), as well as good peaking time in the preamplifier.
- **High Speed:** Associate all hits uniquely with a given 25ns beam crossing. Contributions to this timing come from timewalk in the preamp/discriminator, digital timing on FE chip, clock distribution on module, and relative timing of different modules.
- **Low Power:** Meet these specifications with an analog power budget of about 40μW/channel and a total power budget for the complete FE chip of about 250mW.
- Full Custom design with about 800K transistors to integrate required functions, layout pushes rules to their limits, and still requires circuit design compromises.

Front-end Electronics Prototypes

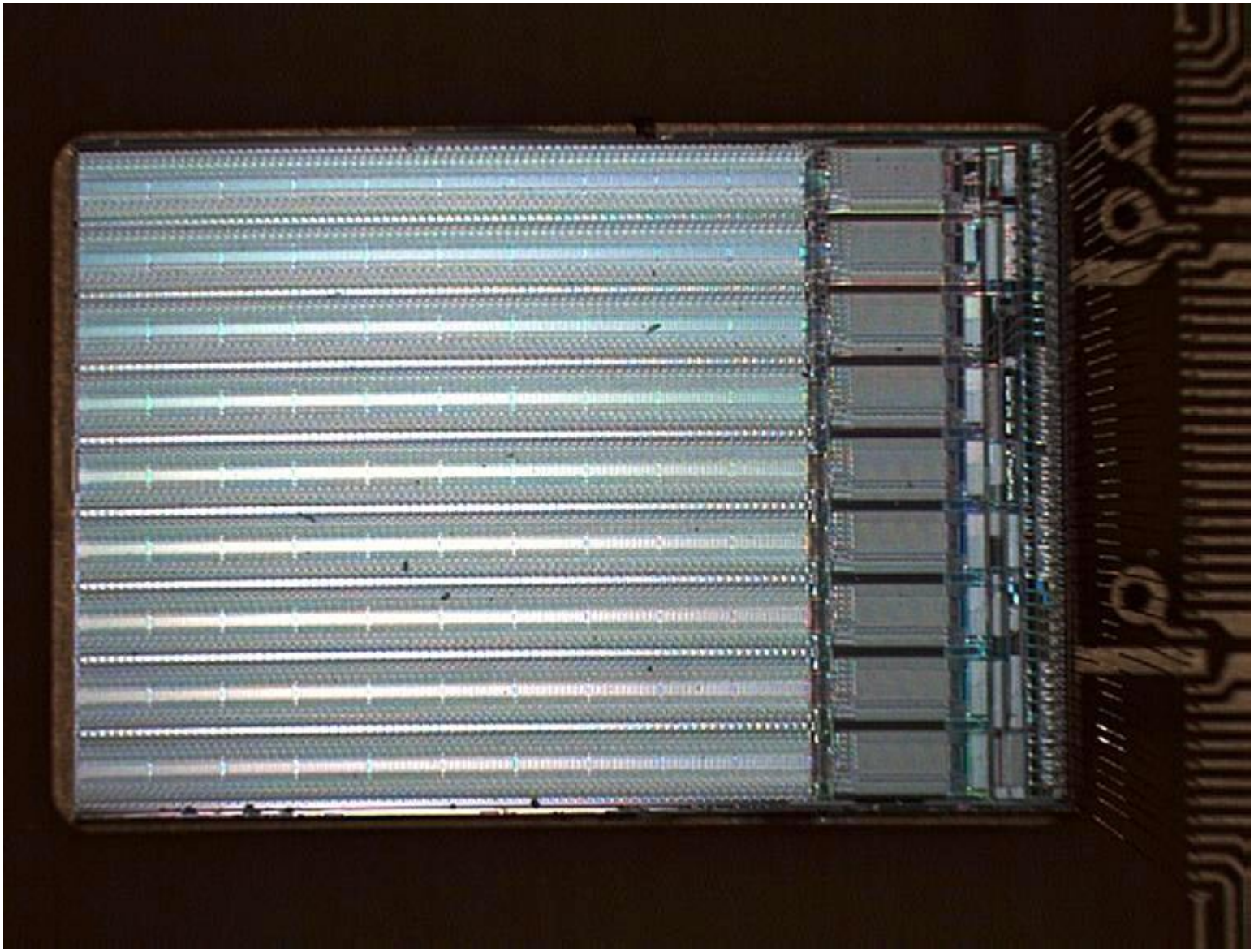
Several generations of prototypes have been built:

- First “proof of principle” chips were built in 96.
- First realistic prototypes were designed in two parallel efforts in 97/98, producing a rad-soft HP prototype (FE-B) and a rad-soft AMS prototype (FE-A/FE-C).
- Prototypes of critical elements made in both rad-hard processes (TEMIC DMILL and Honeywell SOI) to study performance and radiation hardness.
- Have just received first version of a complete DMILL chip (FE-D), and are working on common design Honeywell chip (FE-H). Vendor choice planned in late 2000.

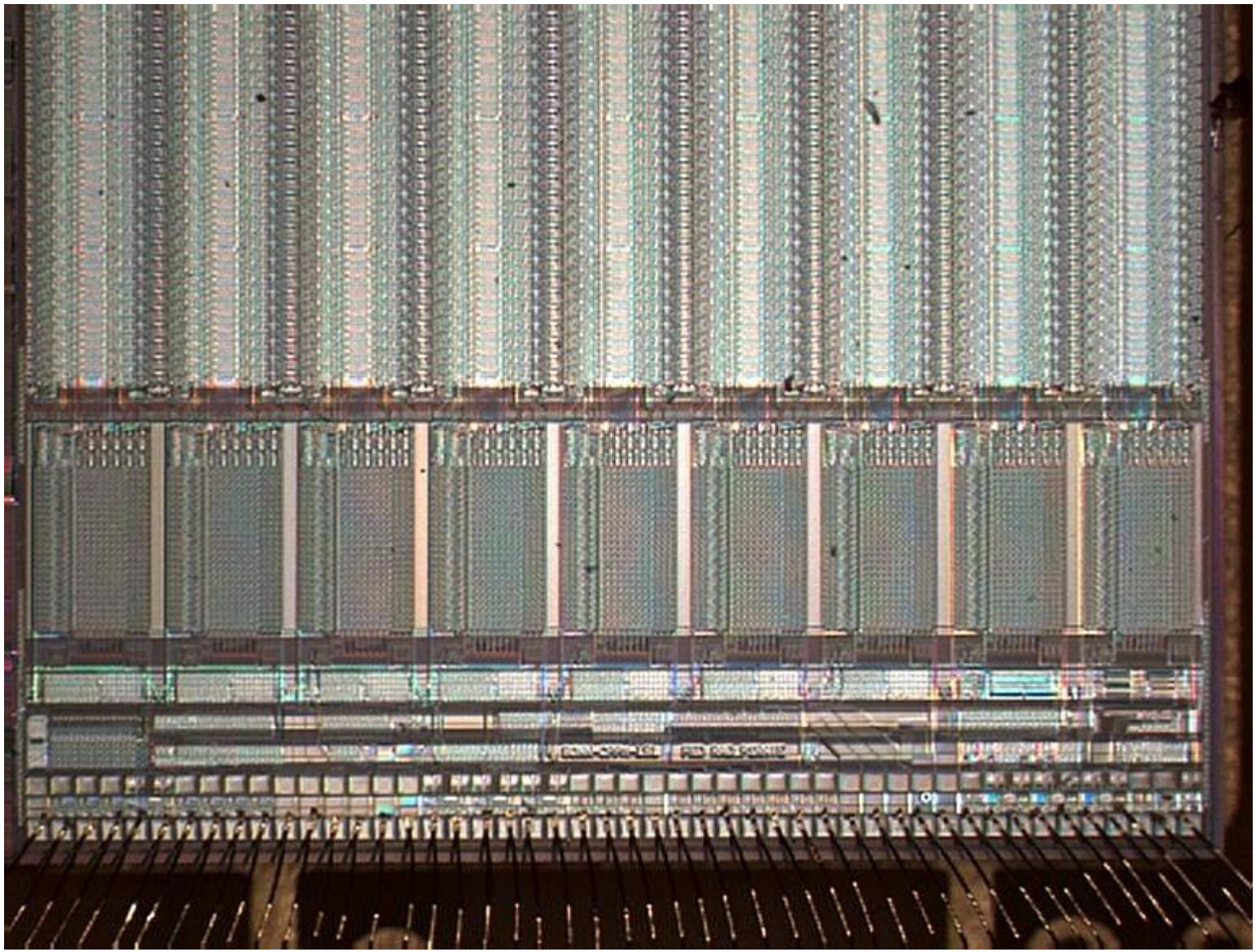
Features of final design:

- Preamplifier provides excellent leakage current tolerance and relatively linear time-over-threshold (TOT) behavior via feedback bias adjustment.
- Discriminator is AC-coupled, and includes 3-bit trim DAC for threshold vernier.
- Readout architecture uses distributed 7-bit timestamp bus, and leading-edge plus trailing-edge latches in each pixel to define times of LE and TE.
- Asynchronous data push architecture used to get data into buffers at the bottom of the chip, where they are stored for the L1 latency, after which they are flagged for readout or deleted. Chip transmits Trigger/Row/Column/TOT for each hit.

FE-D Chip under test:

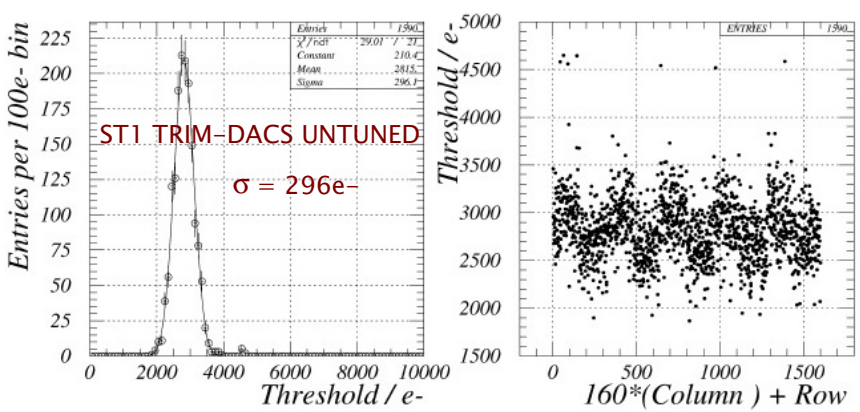


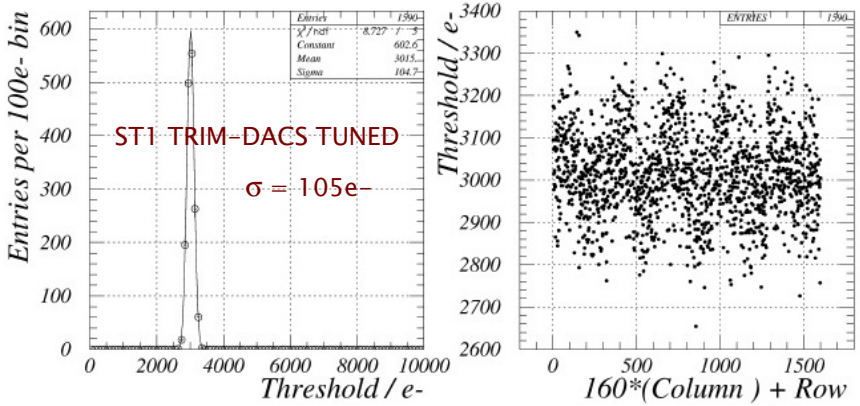
Details of Bottom of Chip:

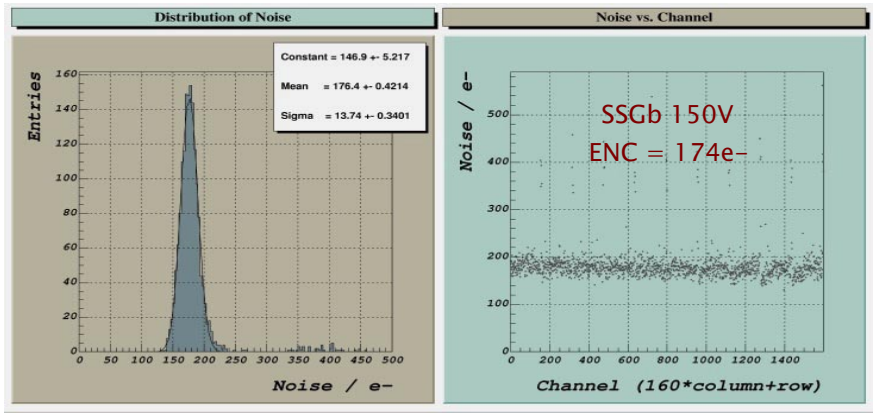


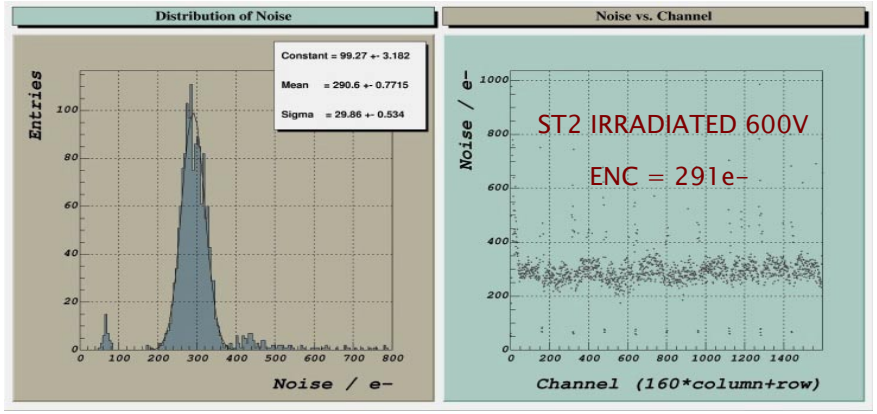
Lab Measurements (NOT with DMILL Chip)

Examples of threshold and noise behavior in single chips:



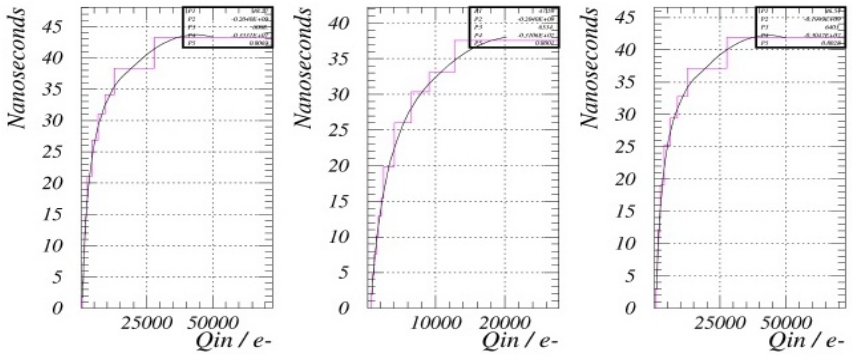


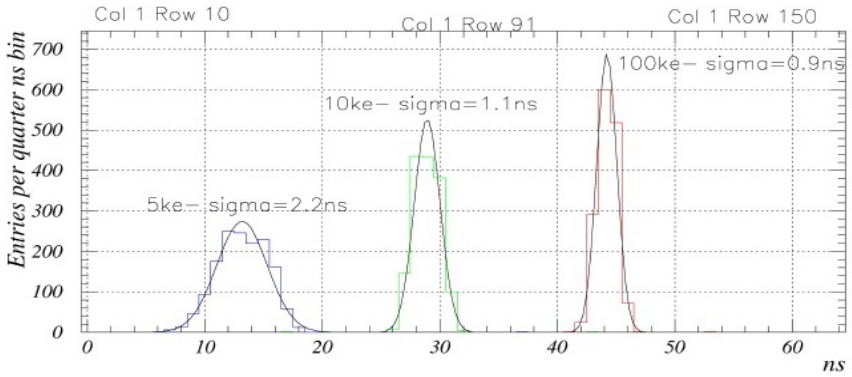




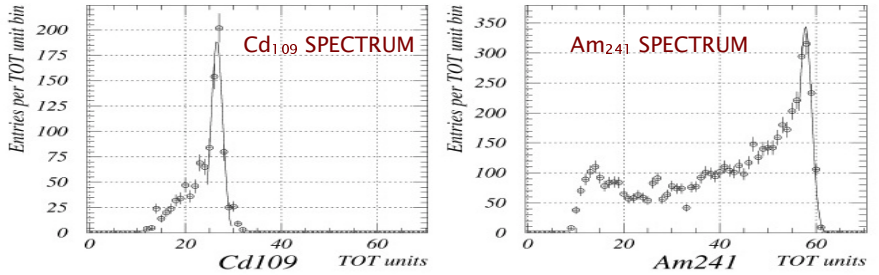
- Using individual Trim DACs, manage to achieve excellent dispersions.
- Measured noise is quite good, even for small-gap design pre-rad, and noise still remains acceptable after irradiation (reduced shaping time and parallel noise from leakage current itself both increase noise).

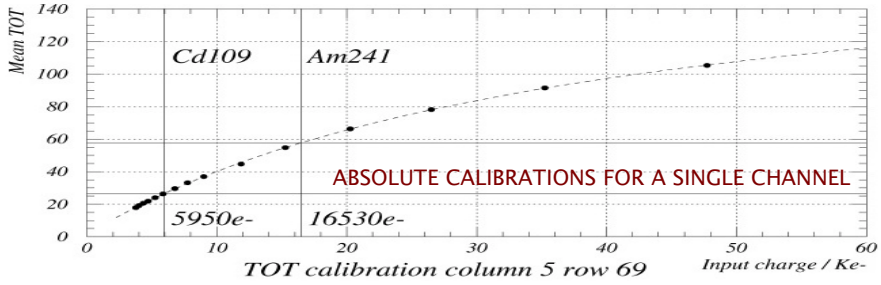
Examples of timing and charge measurements:

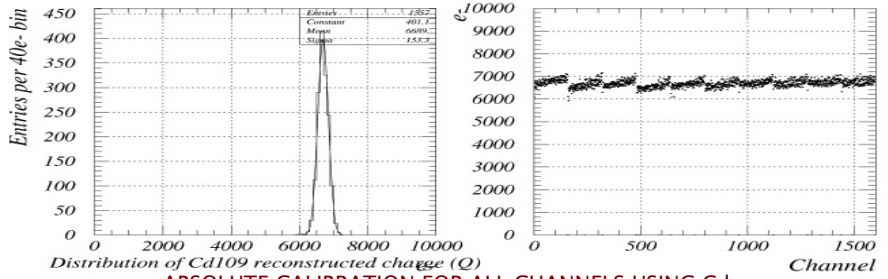




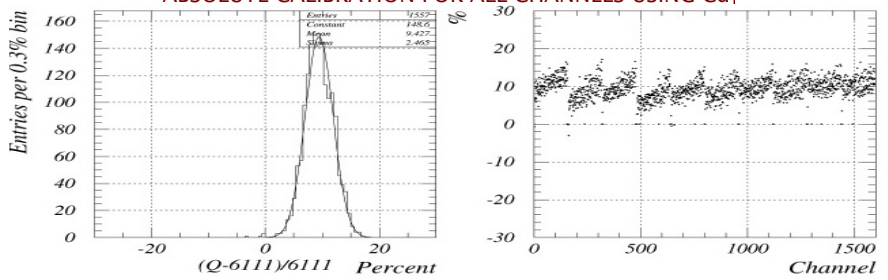
- Timing performance at large charge is excellent, and timewalk is acceptable.
- Charge measurement is high quality, but requires individual calibrations. Uniformity of internal calibration is good.







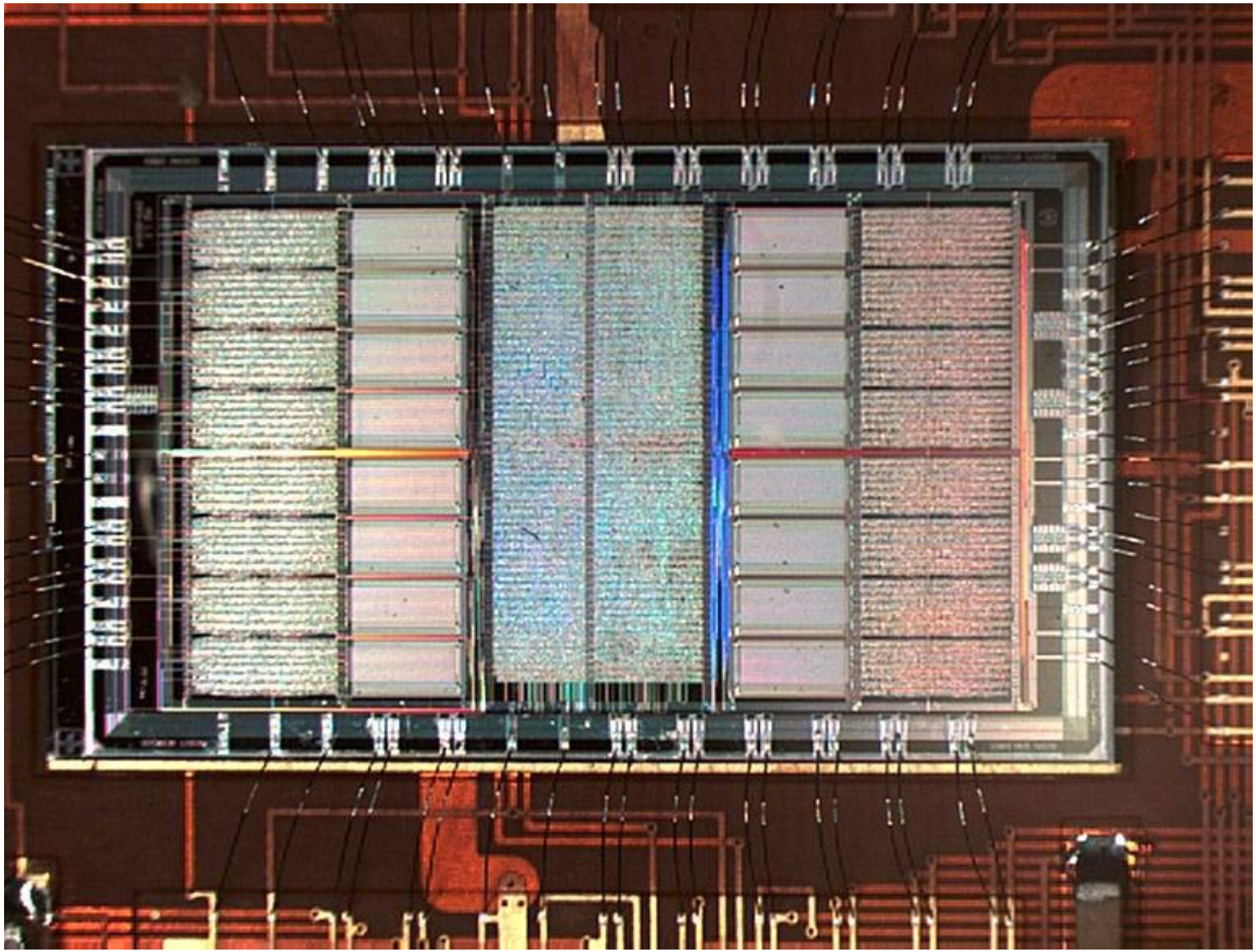
ABSOLUTE CALIBRATION FOR ALL CHANNELS USING Cd_1



Module Controller Chip Prototypes and Issues:

- Significant on-chip buffering required on inputs (16 FIFO's, each 25 bits wide and 32 words deep). These are implemented as full-custom blocks.
- Complex control functions that must be efficiently synthesized from Verilog description using Synopsys.
- This requires a high quality standard cell library in order to achieve good packing and routing density. This library must be well-characterized pre- and post-rad, and it must be possible to back-annotate routing parasitics and establish the expected performance of the full design after final routing. Chip must perform event building on 16 parallel 40Mbit/s input streams in real time as there is no mechanism for flow control on data from FE chips, so timing goals are critical.
- Prototype made in AMS 0.8µ process, using about 400K transistors and a die size of about 80 mm^2.
- All basic functions worked as expected. There are minor improvements underway in the some of the algorithms used by the chip, particularly error handling.
- A partial-scale prototype was made in our recent DMILL run, known as MCC-D0. This included basic blocks such as the FIFO, and command decoder. The intention was to test the DMILL standard cell library and understand the performance of a synthesized design after irradiation.

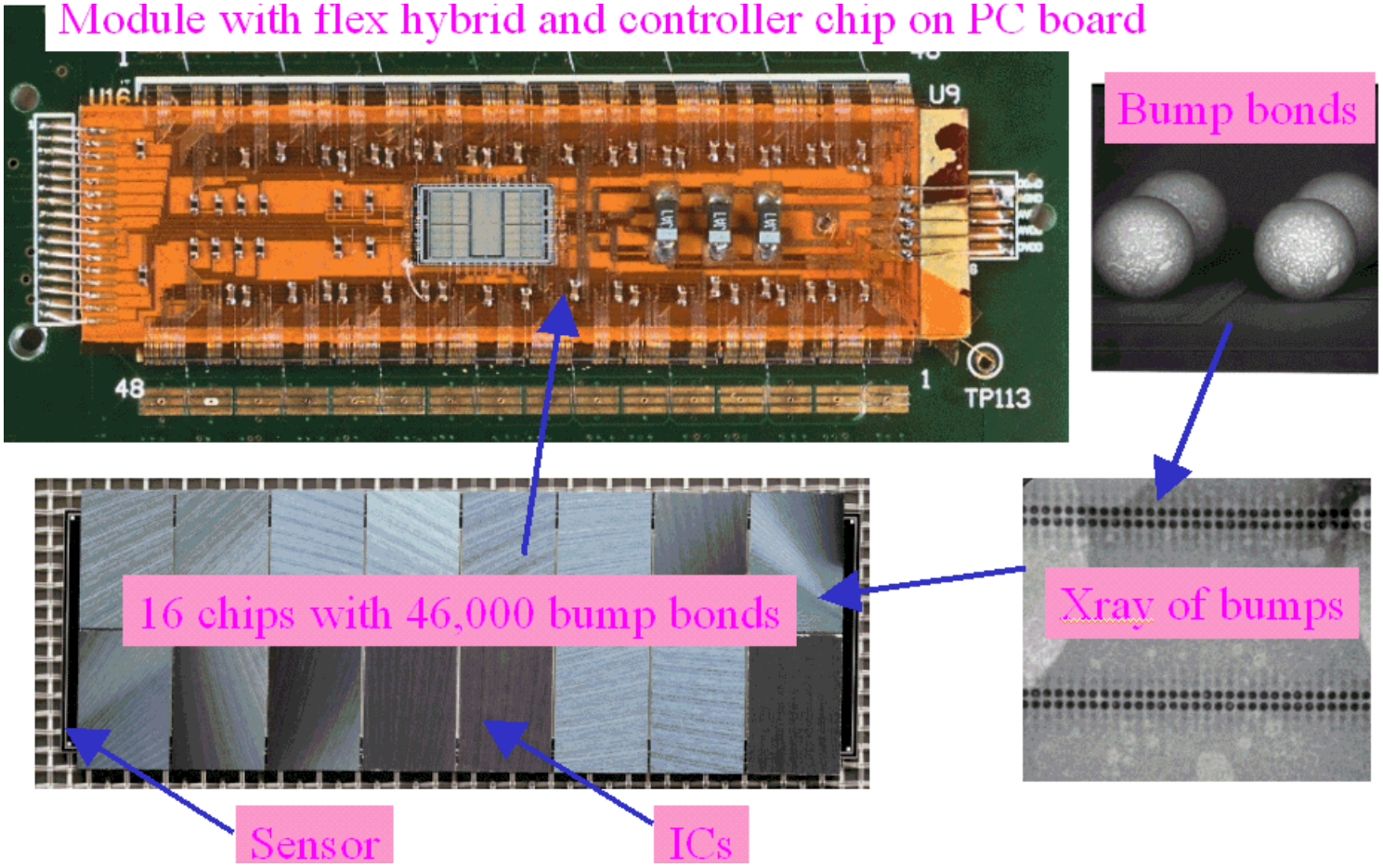
Module Controller Chip prototype in AMS 0.8μ:



Module Issues:

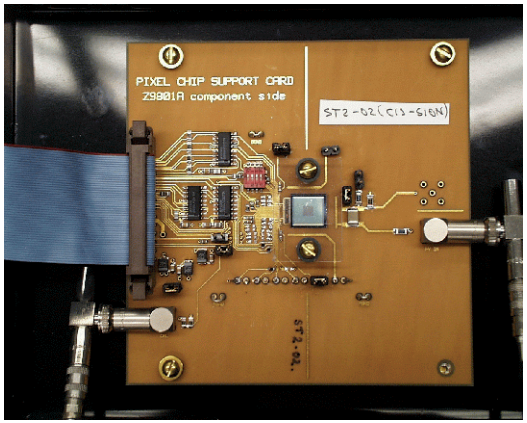
Major issue is interconnection:

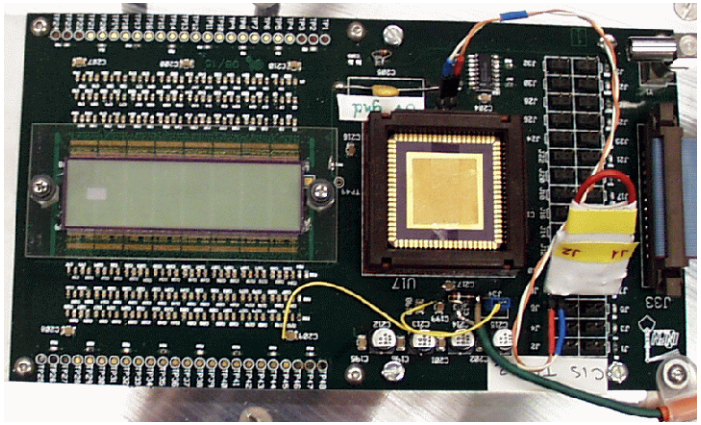
- Connect 46K pixel implants on sensor to preamplifiers in FE electronics chip using bump-bonding technology (50μ pitch is not commercial standard !)
- Connect 16 FE chips with MCC chip and optolink components and power.

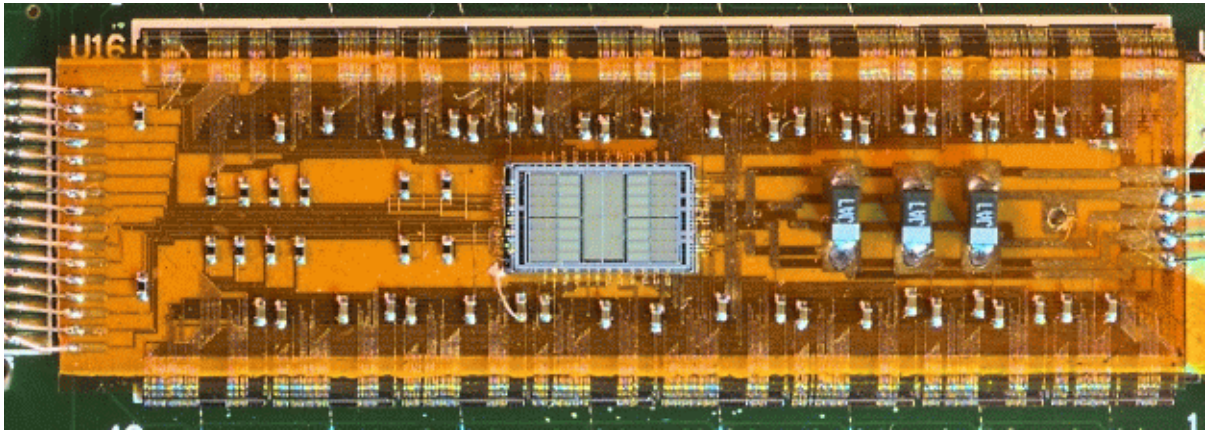


Module Prototyping:

- Built many “single chip” devices using smaller sensors for small-scale studies. Some studies were done with irradiated sensors and rad-soft electronics.
- Built about 10 modules with IZM solder bumps, several as “bare” modules with interconnections on PC board, several as “Flex” modules, others as “MCM-D” modules. Some, but not all, of these modules work very well.







Scope and Schedule of Project

- Total of approximately 2200 modules are required for complete detector. This corresponds to about 35K good FE die after all assembly steps.
- Assuming 38% fab yield (very optimistic), and other assembly yields we know about, we estimate this requires 150K FE die to be fabricated, or approximately 1200 wafers. Outer layers of system are about 1050 wafers of this. About 100 additional wafers would be needed for all of the MCC and Opto-link IC's.
- We need to achieve about 28% yield for the DMILL FE chips to be able to meet our budget (based on frame contract), so yield is of enormous concern to us.
- We submitted our first full-scale prototypes of each of the major IC's in the pixel project for fabrication by TEMIC in Aug. 99. We have been testing these die since the wafers returned in late October. Based on this initial testing, we have identified several design problems, and we believe also some fabrication problems. Addressing these problems is our primary goal for this meeting.
- We plan to submit a second engineering run in about 4-6 weeks time, and a full prototype and irradiation program is planned during a six month evaluation period. These next chips must have high yield and work very well.
- The next step would be a first "pre-production" run in Spring 2001. This would be followed by the series production over the following 18 months or so.
- We are presently building full-scale prototypes with both TEMIC/DMILL and Honeywell/SOI, in order to find the optimal solution for ATLAS pixels.